C8051F226

25 MIPS, 8 kB Flash, 8-Bit ADC, 48-Pin Mixed-Signal MCU

Analog Peripherals

8-Bit ADC

- ±1/2 LSB INL; no missing codes
- Programmable throughput up to 100 ksps
- 32 external inputs (each port I/O can be configured as an ADC input on-the-fly)
- Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
- Data-dependent windowed interrupt generator
- V_{REF} from external pin or V_{DD}

Two comparators

- Programmable hysteresis
- Configurable to generate interrupts or reset

V_{DD} Monitor and Brown-out Detector

On-Chip JTAG Debug

- On-chip emulation circuitry facilitates full-speed, non-intrusive, in-circuit emulation
- Supports breakpoints, single stepping, watchpoints, inspect/modify memory, and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Fully compliant with IEEE 1149.1 specification

High-Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instructions in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz system clock
- Expanded interrupt handler; up to 21 interrupt sources

Memory

- 1280 bytes data RAM
- 8 kB Flash; in-system programmable in 512 byte sectors (512 bytes are reserved)

Digital Peripherals

- 32 port I/O; all are 5 V tolerant
- Hardware SPI™ and UART serial ports available concurrently
- 3 general-purpose 16-bit counter/timers
- Dedicated watchdog timer; bidirectional reset

Clock Sources

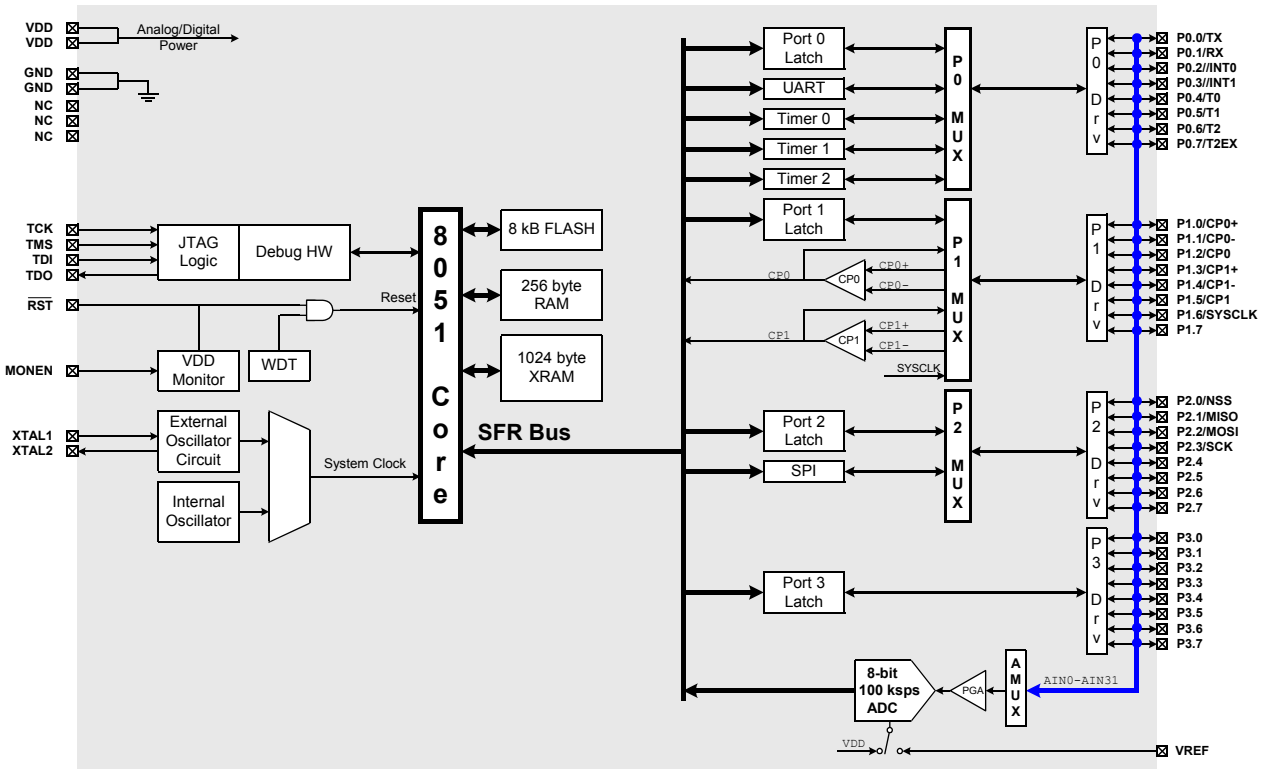
- Internal programmable oscillator: 2–16 MHz
- External oscillator: Crystal, RC, C, or Clock
- Can switch between clock sources on-the-fly

Supply Voltage: 2.7 to 3.6 V

- Typical operating current: 9 mA at 25 MHz
- Typical stop mode current: <0.1 uA

48-Pin TQFP

- **Temperature Range: –40 to +85 °C**

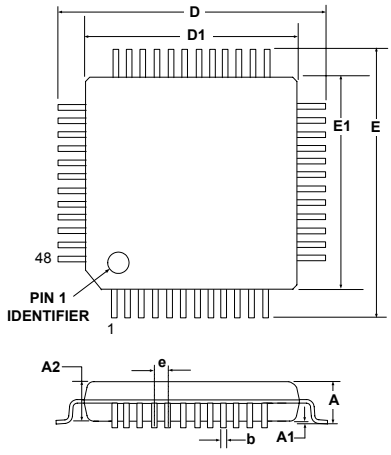


Selected Electrical Specifications

(T_A = –40 to +85 C°, V_{DD} = 2.7 V unless otherwise specified unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL CHARACTERISTICS					
Digital Supply Voltage		2.7		3.6	V
Digital Supply Current with CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz; V_{DD} Monitor Disabled		9 0.4 11		mA mA µA
Digital Supply Current (shutdown)	Oscillator not running; V_{DD} Monitor Enabled Oscillator not running; V_{DD} Monitor Disabled		7 0.1		µA µA
Digital Supply RAM Data Retention Voltage			1.5		V
CPU & DIGITAL I/O PORTS					
Clock Frequency Range		DC		25	MHz
Port Output High Voltage	I_{OH} = –3 mA, Port I/O push-pull	V_{DD} – 0.7			V
Port Output Low Voltage	I_{OL} = 8.5 mA			0.6	V
Input High Voltage		0.8 x V_{DD}			V
Input Low Voltage				0.2 x V_{DD}	V
SPI Bus Clock Frequency	fCLK=MCU Clock; SPI in Master Mode			fCLK/2	MHz
A/D CONVERTER					
Resolution		8			bits
Integral Nonlinearity				±1/2	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1/2	LSB
Signal to Noise Ratio			49		dB
Throughput Rate				100	ksps
Input Voltage Range		0		V_{REF}	V
COMPARATORS					
Response Time	| CP+ – CP- | = 100 mV		4		µs
Input Voltage Range		–0.25		V_{DD} + 0.25	V
Input Bias Current		–5	0.001	+5	nA
Input Offset Voltage		–10		+10	mV

Package Information



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	9.00	-
D1	-	7.00	-
e	-	0.50	-
E	-	9.00	-
E1	-	7.00	-

C8051F226DK Development Kit